

DETAILED ACTION

1. This communication is in response to the amendment filed 10/06/2009 in which claims 1 and 13 were amended, claims 14 and 15 were added and claim 12 was cancelled.
2. Claims 1, 3, 6, 7, 11, and 13-15 are currently pending.

EXAMINER'S AMENDMENT

3. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Takashi Saito (L0123) on 7 January 2010.

The application has been amended as follows:

Claim 1, line 20, insert –physical– in between “in” and “contact”;

Claim 15, line 1, insert –1– in between “claim” and “wherein”.

REASONS FOR ALLOWANCE

4. Claims 1, 3, 6, 7, 11, and 13-15 are allowed over the prior art of record.
5. The following is an examiner's statement of reasons for allowance: The prior art fails to teach in combination a solid state imaging apparatus comprising a first silicon layer made of silicon having the first conductivity type formed in a region of the silicon substrate, and forming the bottom and sidewalls of the isolation trench, and a second silicon layer made of silicon having the first conductivity type in contact with a bottom

side of the first silicon layer, wherein an impurity concentration of the second silicon layer is less than that of the first silicon layer, and the second silicon layer is in physical contact with a side surface of the first semiconductor layer, and including all limitations.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yoshiko (JP 2004-039832) discloses a first silicon layer 6 and a second silicon layer 11, wherein layer 11 has a lower impurity concentration than 6; however, 11 is not in physical contact with the first semiconductor layer 18.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph C. Nicely whose telephone number is (571) 270-3834. The examiner can normally be reached on Monday through Friday 7:30AM-5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Landau can be reached on (571) 272-1731. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Joseph C. Nicely/
Examiner, Art Unit 2813

/Matthew C. Landau/
Supervisory Patent Examiner, Art
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